Experimental Validation of an Iterative Receiver for Energy-Efficient Communications

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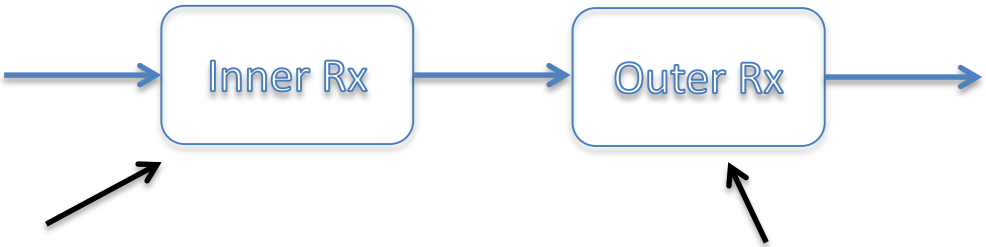
Background

- Wireless connectivity anytime, anywhere, anything
- Powerful error correcting codes make communication possible even at low SNRs



Apply DSP and estimation theory for

- Repairing several signal distortions
- Synchronization (timing, frequency and phase)
- Channel estimation and equalization

Detector and decoder with input samples perturbed by AWGN only

$$r = s + n$$

Acquisition Approaches

	Benefits	Drawbacks	Suitable for
Data-aided	Accuracy	Low Spectral Efficiency	Burst mode
Decision-directed	Utilize Rx decisions	Error propagation	High SNR
Non-data-aided	High spectral efficiency	Slow convergence	Continuous mode
Code-aided	➢ Accuracy ➢ High spectral efficiency	Complexity	Soft decoder

Iterative Rx

- At high SNR, conventional approaches perform well
- At low SNR, acquisition is difficult as the signal is not clearly differentiated from noise
  - Data-aided algorithms prove costly for bandwidth
  - Decision-directed approach is unreliable
  - Non-data-aided techniques simply fail to work in general
- One way to reduce the noise is significant averaging
  - Utilization of soft decisions from decoders = Iterative Rx

Motivation - 1

- Squeeze the maximum amount of information from the received samples before quantization
- Viterbi[1] summarized the essence of Shannon theory for digital communications in the form of three lessons
- The first lesson was
  - "Never discard information prematurely that may be useful in making a decision until after all decisions related to that information have been completed"
- This lesson lead to
  - Wireless systems: FEC with soft decision decoding
  - Wireline modems: ML sequence estimation

[1] Wireless Digital Communication: A View Based on Three Lessons Learned, IEEE Communications Magazine, Vol. 29, No. 9, 1991

Motivation - 2

Iterative Processing Scope
Carrier phase synchronization
Timing synchronization
Channel estimation
Joint phase and frequency synchronization
Joint phase and timing synchronization
Joint frequency and channel estimation
Joint timing, frequency and channel estimation

- Common theme is constructing soft symbols from the LLRs provided by the decoder and use them as known data
- All research is based on individually useful schemes but not on how they fit together within a larger framework

LLR = Log Likelihood Ratio

Motivation - 3

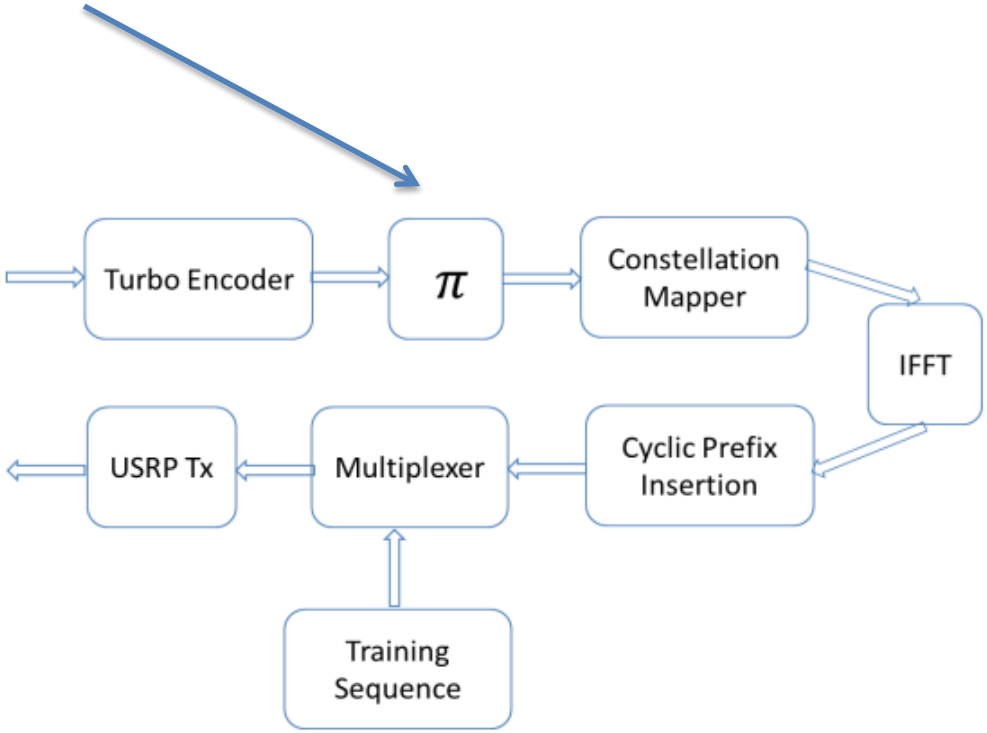
- All the publications on this topic are based solely on simulation results
- An experimental demonstration is necessary to validate them
- In words of Klein Gilhousen, co-Founder of Qualcomm Inc.
  - "If you haven't tested it, it doesn't work"

Contributions

- Physical demonstration of an iterative receiver structure using experimental hardware (USRP B210) – it works
- Simultaneous effects of major impairments including
  - Timing synchronization
  - Carrier frequency synchronization
  - Channel estimation and equalization
  - Algorithm partition for manageable delay and complexity
- Alternative approach for carrier frequency synchronization that eliminates the need of bringing the frequency correction within the iterative loop

Tx

- Interleaver is very important to make bits appear independent at the Rx



Rx

- We define three criteria
  1. Computational complexity should not be prohibitive
  2. Any operation inside the iterative loop has to be simple
  3. Avoid the sensitivity of iterative algorithms to initialization
  4. Iterative structure should not limit frequency offset range
- Conclusions based on these criteria

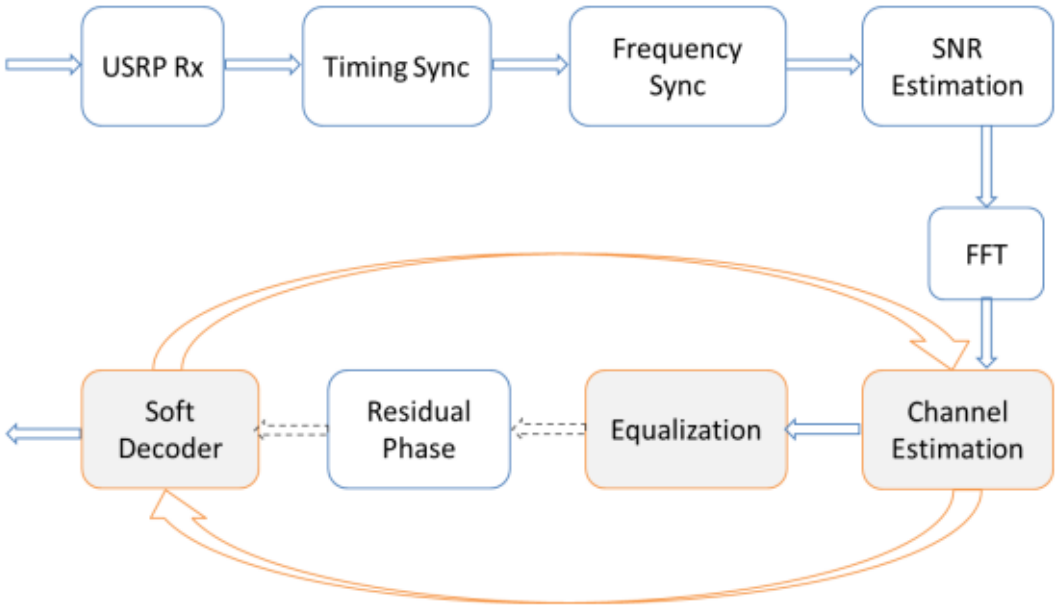
  1+2. Timing synchronization cannot be done iteratively

  3. A short training sequence can be used at the start

  4. Soft symbols in estimating the frequency offset constrain the capture range within a very narrow margin

  -- This leaves the channel estimator and equalizer embedded within the turbo loop

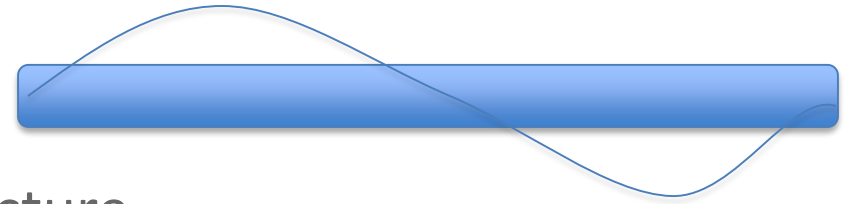
Rx



- Before the first iteration, any residual phase offset arising from remaining frequency offset is removed
- Iterations between the soft decoder, channel estimation and equalizer are executed

Residual CFO Correction

- Residual carrier frequency offset (CFO) needs to be corrected before the iterations start
  - Low SNR
  - Long frame lengths



- Utilize the block based structure
- A frequency offset ϵ rotates the frequency domain symbols by a time-variant phasor $e^{j2\pi\epsilon \cdot g(L) \cdot n}$
- Phase increment from one symbol to the next is given by

$$\theta = 2\pi\epsilon \cdot g(L)$$

- Can be corrected on a symbol by symbol basis

g(L) is a function of block length L

Iterative Processing

- The soft symbols $\hat{X}_k^{(q)}$ are constructed as

$$\hat{X}_k^{(q)} = \sum_{a_i,b_i} P_{a_i}^{(q)} P_{b_i}^{(q)} Z_{a_i,b_i}$$

$$= \tanh\left(\frac{LLR(a_i)}{2}\right) + j \cdot \tanh\left(\frac{LLR(b_i)}{2}\right)$$

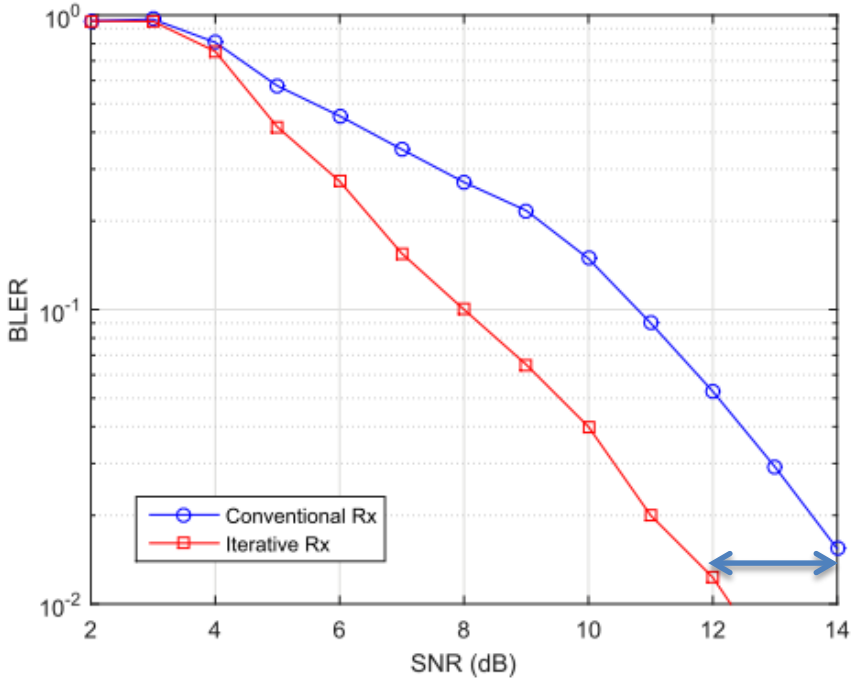
where

  - a_i and b_i are two bits mapped to i^{th} QPSK symbol Z_{a_i,b_i}
  - $P_{a_i}^{(q)}$ and $P_{b_i}^{(q)}$ are their a posteriori probabilities in q^{th} iteration
  - LLR is the log likelihood ratio

$$LLR(a_i) = \log \frac{\Pr(a_i = +1|\mathbf{r})}{\Pr(a_i = -1|\mathbf{r})}$$

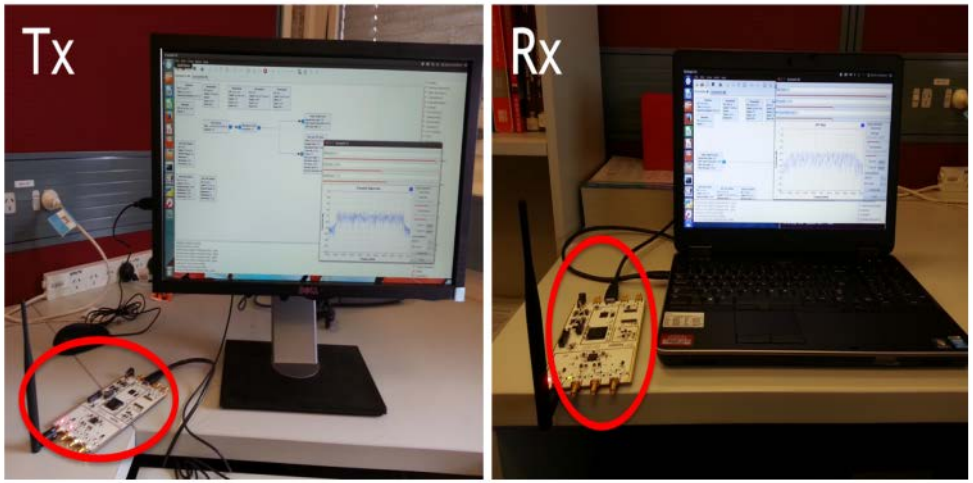
Simulation Results

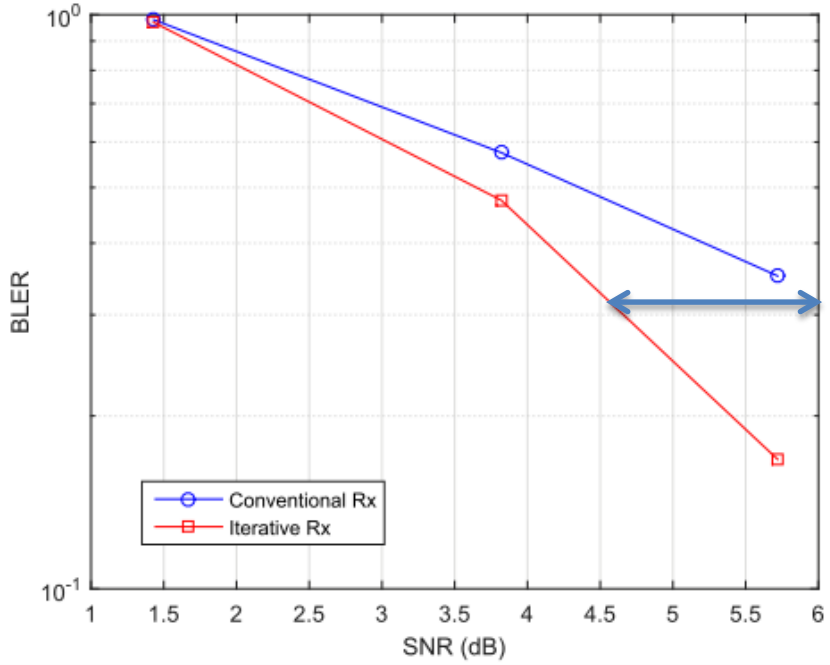
- Frame length of 1500 bits
- QPSK modulation
- Code rate ½
- RSC generators $(13)_8$ and $(15)_8$
- Proakis channel B
- Gain is around 2 dB



Experimental Results

- USRP B210
- 2.4 GHz ISM band
- Bandwidth - 8 MHz
- FFT size - 64
- CP size - 16
- Modulation - QPSK
- Code rate - ½
- Training size - 128
- Gain is around 1.5 dB





Conclusions and Future Work

- Experimental results were found to be in close agreement with simulations in previous publications
- Differences can arise due to
  - Code rate, generator polynomials, constraint length
  - Number of iterations
  - Assumptions
- Drawback: Need LLRs for parity bits as well adding complexity
  - Devised a technique that works with information bits only
- 1.5-2 dB gain is good enough to warrant its adoption in products